IN THE SPECIFICATION

Please replace the following paragraphs:

Page 3, paragraphs [0007] to [0012].

[0007] FIG. 1 is a block diagram of an embodiment of the disclosed information handling system.

[0008] FIG. ~~2A~~ 2a is a current vs. time graph illustrating the amount of current supplied over time by battery 215 of FIG. 1.

[0009] FIG. ~~2B~~ 2b is a current vs. time graph illustrating the amount of current supplied over time by battery 220 of FIG. 1.

[0010] FIG. ~~2C~~ 2c is a current vs. time graph illustrating the aggregate amount of current supplied over time by both batteries 215 and 220 of FIG. 1.

[0011] FIG. ~~3A~~ 3a is a voltage vs. time graph illustrating the switching circuit 210's effect on level of voltage supplied to system board 200 of FIG 1.

[0012] FIG. ~~3B~~ 3b is a voltage vs. time graph illustrating the effect of capacitor 235 on the level of voltage supplied to system board 200 of FIG. 1.

Page 3 to page 4, paragraph [0013].

[0013] For purposes of this disclosure, an information handling system (IHS) may include any instrumentality or aggregate of instrumentalities operable to compute, classify, process, transmit, receive, retrieve, originate, switch, store, display, manifest, detect, record, reproduce, handle, or utilize any form of information, intelligence, or data for business, scientific, control, or other purposes. For example, an information handling system may be a personal computer, a network storage device, or any other suitable device and may vary in size, shape, performance, functionality, and price. The information handling system may include random access memory (RAM), one or more processing resources such as a central processing unit (CPU) or hardware or software control logic, ROM, and/or other types of nonvolatile memory. Additional components of the information handling system may include one or more disk drives, and one or more network ports for communicating with external devices as well as various input and output (I/O) devices, such as a keyboard, a mouse, and a video display. The information handling system may also include one or more buses operable to transmit communications between the various hardware components.

Page 4, paragraph [0014].

[0014] In one embodiment, an information handling system 100, Fig. 1, includes system board 200. System board 200 includes a processor 105 such as an Intel Pentium series processor or one of many other processors currently available. An Intel Hub Architecture (IHA) chipset 110 provides IHS ~~system~~ 100 with graphics/memory controller hub functions and I/O functions. More specifically, IHA chipset 110 acts as a host controller which communicates with a graphics controller 115 coupled thereto. A display 120 is coupled to graphics controller 115. Chipset 110 further acts as a controller for main memory 125 which is coupled thereto.

Chipset 110 also acts as an I/O controller hub (ICH) which performs I/O functions. A super input/output (I/O) controller 130 is coupled to chipset 110 to provide communications between chipset 110 and input devices 135 such as a mouse, keyboard, and tablet, for example. A universal serial bus (USB) 140 is coupled to chipset 110 to facilitate the connection of peripheral devices to system 100. System basic input-output system (BIOS) 145 is coupled to chipset 110 as shown. BIOS 145 is stored in CMOS or FLASH memory so that it is nonvolatile.

Page 5, paragraph [0017].

[0017] More particularly, IHS 100 includes a switching circuit 210 coupled to battery 215, battery 220 and main power input 200A of system board 200. As discussed in more detail below, a function of switching circuit 210 is to repeatedly switch main power input 200A of system board 200**[[-]]** between battery 215 and battery 220. To achieve this end, switching circuit 210 includes switching transistors 216 and 217 connected as shown. Switching transistor 216 is series coupled between battery 215 and main power input 200A via diode 225. Switching transistor 217 is series coupled between battery 220 and main power input 200A via diode 230. The respective gates of switching transistors 216 and 217 are coupled to switching signal generator 218. Switching signal generator 218 generates a switching signal which alternately turns switching transistor 216 on, while switching transistor 217 is off, and turns switching transistor 217 on, while switching transistor 216 is off. In one embodiment, the switching rate of the switching signal generated by switching circuit 218 is a rate within the range of approximately 100 KHz to approximately 500 KHz, although different switching rates are suitable in other embodiments.

Page 7 to page 8, paragraph [0023].

[0023] As indicated by dashed line 208, at all given points in time indicated in FIG. 2a, battery 215 supplies X amount of current under a continuous load. However, as indicated by solid line 206, battery 215 supplies 2X amount of current for some periods of time but supplies no (0) amount of current for other periods of time. The periods of time during which battery 215 supplies 2X amount of current represents the periods of time during which switching circuit 210_1 depicted in FIG. 1, has connected battery 215 for supplying power to system board 200. Accordingly, the periods of time during which battery 215 supplies no current represents the periods of time during which switching circuit 210 has connected another battery (i.e. battery 220) for supplying power to system board 200.

Page 8, paragraph [0025].

[0025] As indicated by dashed line 218, at all given points in time shown in FIG. 2b, battery 220 supplies X amount of current under a continuous load. However, as indicated by solid line 216, battery 220 supplies 2X amount of current for some periods of time and supplies no (0 amount) current for other periods of time. The periods of time during which battery 220 supplies 2X amount of current represents the periods of time during which switching circuit 210 depicted in FIG. 1, has connected battery 220 for supplying power to system board 200. Accordingly, the periods of time during which battery 220 supplies no current represents the periods of time during which switching circuit 210 has connected another battery (i.e. battery 215) for supplying power to system board 200. Referring now simultaneously to $FIG._2$a and $FIG._2$b, it can be seen that during the periods where battery 215 supplies current, battery 220 supplies no current, and vice versa.

Page 9, paragraph [0027].

[0027] As indicated by dashed line 228, at all given points in time shown in FIG. 2c, multiple batteries (such as batteries 215 and 220) in an existing IHS, supplies X amount of current. However, as indicated by solid line 226, batteries 215 and 220 in the illustrative embodiment are discharged together and accordingly supplies approximately 2X amount of current at all given moments of time shown in FIG. 2c. Accordingly, in the illustrative embodiment, the amount of power supplied to system board 200 is also approximately twice the amount of power supplied using existing techniques.

Page 9, paragraph [0028].

[0028] FIGs. 3a and 3b are voltage vs. time graphs illustrating the level of voltage supplied to system board 200 over time by batteries 215 and 220. For explanatory purposes, batteries 215 and 220 each supply different levels of voltage. Accordingly, in such a case, repeatedly switching between battery 215 and battery 220 for supplying current and power to system board 200 causes fluctuations in the level of voltage supplied to system board 200.